CMS8F003 Datasheet

Enhanced flash memory 8-bit CMOS microcontrollers

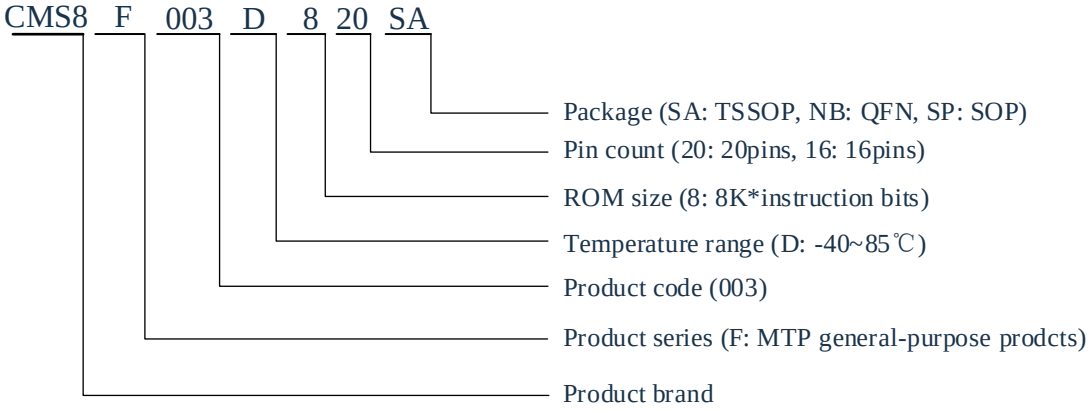
Rev. 0.9.5

1. Product Features

1.1 Features

- **Compatible with MCS-51 instruction set**
  - Fastest machine cycle supports $2T_{SYS}$ @ F_{SYS} ＝16MHz
- **Memory**
  - Program Flash: 8Kx8
  - Universal RAM: 256x8
  - Universal XRAM: 256x8
  - Data Flash: 128x16
- **Oscillation modes**
  - HSI internal high-speed RC oscillation:16MHz
  - HSE external high-speed crystal oscillation: Max.16MHz
  - LSI internal low-speed RC oscillation: 32KHz
- **Interrupt sources**
  - 2 timer interrupts
  - GPIO interrupts
  - Other peripheral interrupts
- **Timers**
  - WDT (Watch Dog Timer)
  - 8-bit timer: TIMER0
  - 16-bit timer: TIMER1
- **PWM**
  - 5-channel PWM
  - Supports complementary mode
  - 4 PWM channels share the same period, independent duty cycle
  - 1 PWM channel with independent period and duty cycle
- **Operating voltage range:**
  - VLVR2~5.5V@16MHz 2T
- **Operating temperature range:**
  - -40℃~85℃
- **Low voltage reset function (LVR)**
  - 1.8V/2.0V/2.5V/3.0V
- **Comparator module**
- **Communication modules**
  - I^2C communication module
  - USART communication module
  - SPI communication module
- **High-precision 12-bit ADC**
  - Internal high-precision 1.2V reference voltage
  - ±1.5% @VDD=2.5V~5.5V T_A=25℃
  - ±2% @VDD=2.5V~5.5V T_A=-40℃~85℃
- **Low power modes**
  - Idle mode (IDLE)
  - Sleep mode (STOP)
- **Supports two-wire/single-wire serial programming and debugging**

1.2 Product Model List



Description

Product	ROM	RAM	Pro EE	I/O	ADC	USART	SPI	IIC	PACKAGE
CMS8F003D816SP	8Kx8	512x8	128x16	14	12Bitx18	1	1	1	SOP16
CMS8F003D820SA	8Kx8	512x8	128x16	18	12Bitx18	1	1	1	TSSOP20
CMS8F003D820NB	8Kx8	512x8	128x16	18	12Bitx18	1	1	1	QFN20

Remark: ROM - Program Memory, Pro EE - Program EEPROM

2. System Overview

2.1 Brief Introduction

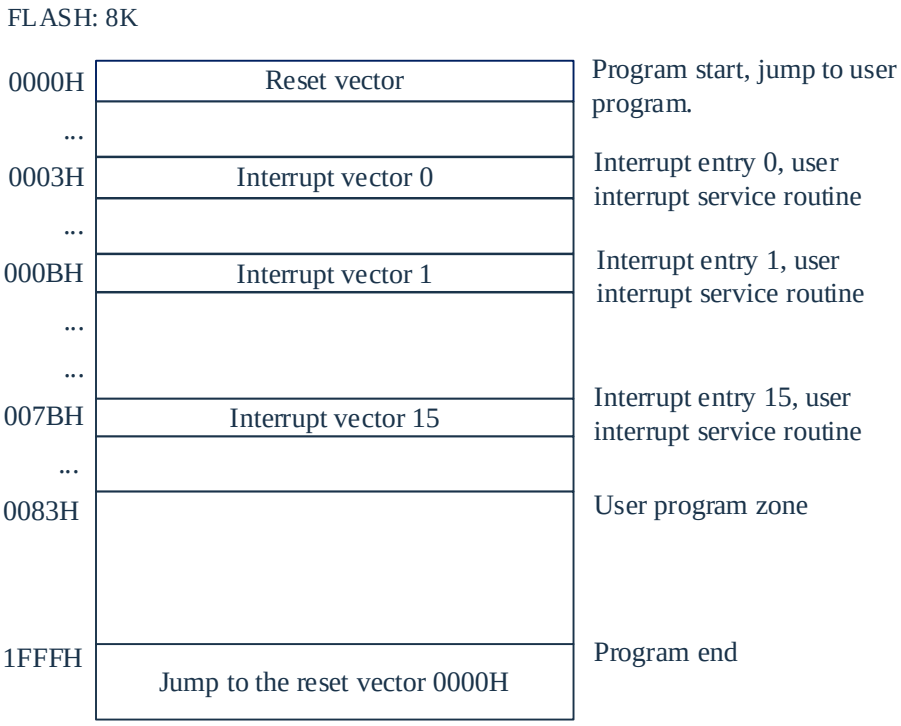
The CMS8F003 series is an 8-bit chip with general-purpose I/O capabilities, featuring an 8051 core and compatible with the MCS-51 2T instruction system. Its maximum operating frequency is up to 16 MHz. The MCU has the following features:

- 8KB program memory, 256B RAM, 256B XRAM, and 128B data memory.
- Three oscillation modes for more flexible clock selection.
- Supports three working modes: Normal, Idle, and Sleep, effectively reducing power consumption.
- Built-in protection features such as Low Voltage Reset (LVR) and Watchdog Overflow Reset, improving system reliability.
- Multiple interrupt sources, including external interrupts, timer interrupts, and other peripheral interrupts, enabling timely response to external events and improving MCU utilization.
- Digital functions can be mapped to any I/O pin.
- 2 timers capable of performing functions like timing, counting, input capture, and output compare.
- 5 channels of 10-bit PWM, which can be configured as 4 channels with shared periods and independent duty cycles + 1 channel for independent output, or 2 complementary output pairs + 1 independent output.
- Communication modules include IIC, SPI, and USART, allowing data transfer between the system and other devices.
- High-precision 12-bit ADC with selectable internal reference voltage, and each I/O pin can serve as an ADC input channel, providing rich analog functionality.

2.2 Memory Structure

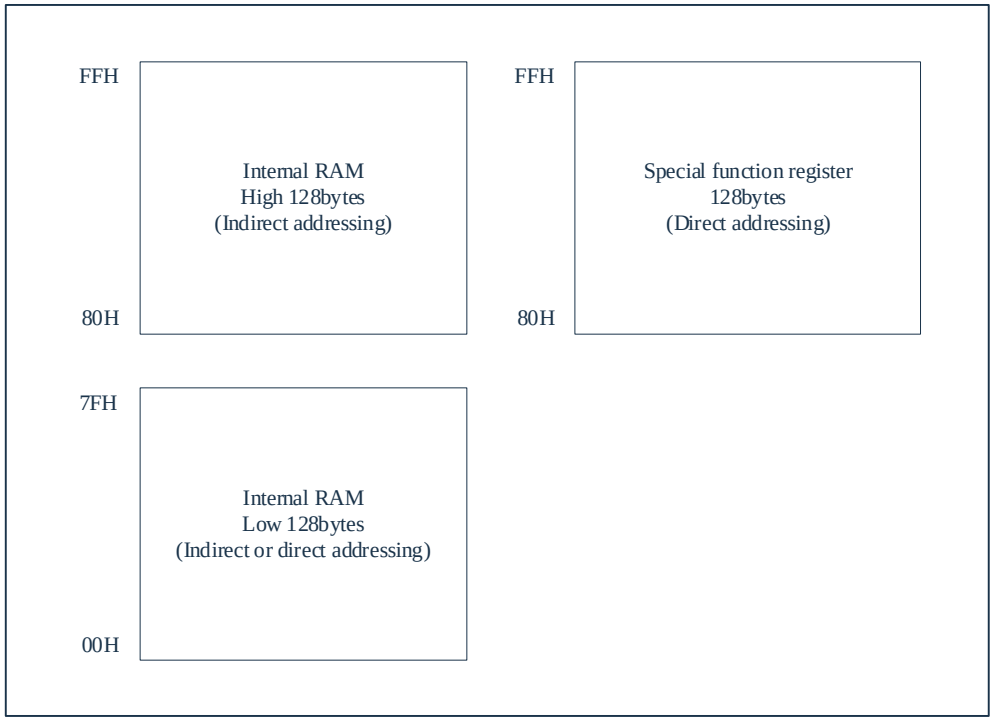
2.2.1 Program Memory (FLASH)

The chip has an 8KB FLASH memory, and the memory allocation block diagram is as follows:

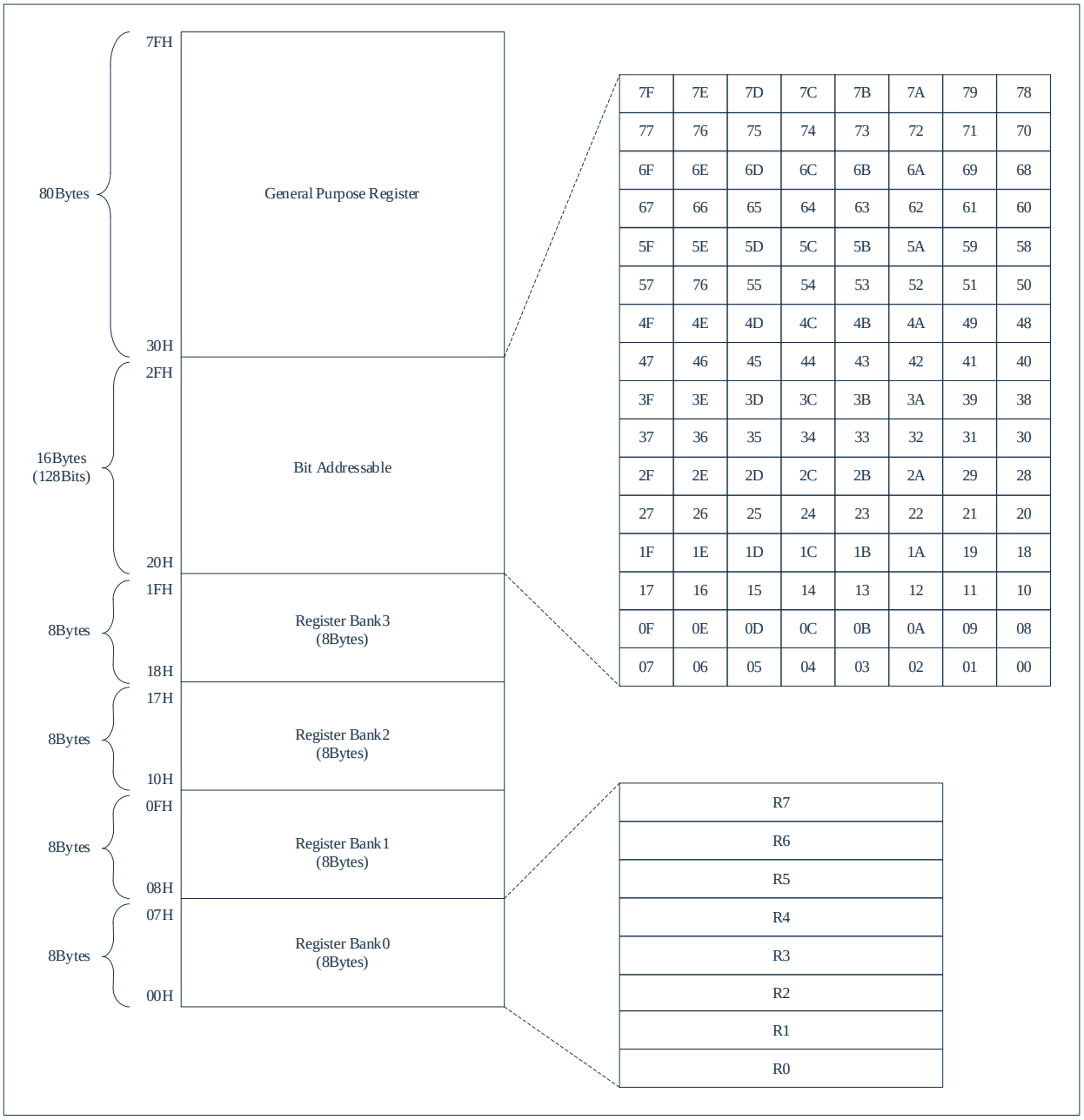


2.2.2 Internal Data Memory (RAM)

The internal data memory is divided into three parts: Low 128 Bytes, High 128 Bytes, and Special Function Registers (SFR). The RAM space allocation structure is illustrated in the diagram below:

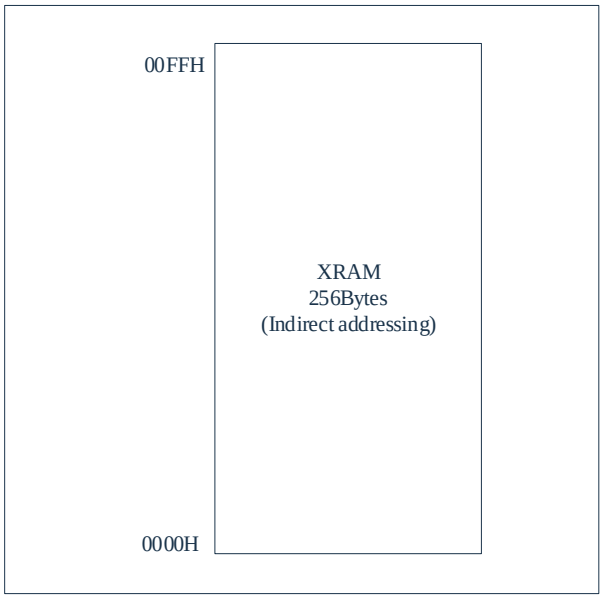


The register allocation of the lower 128 bytes of space, as shown in the diagram above, is as follows: The lowest 32 bytes (00H~1FH) form 4 register groups, each with 8 storage units numbered R0~R7, used to store operands and intermediate results. After a reset, group 0 is selected by default. If other register groups are selected, the program state must be changed to determine the selection. The 16 bytes following the register groups (20H~2FH) form a bit-addressable memory space, where each RAM unit can be accessed by byte or manipulated bit by bit. The remaining 80 storage units (30H~7FH) can be used by the user to set up the stack zone and store intermediate data.



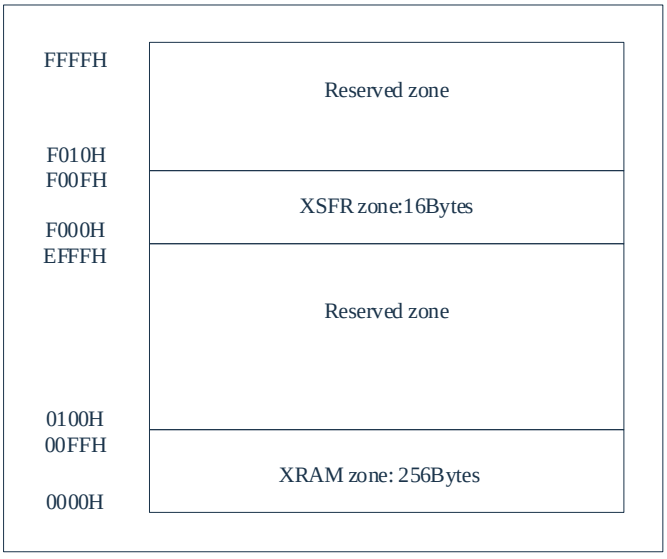
2.2.3 External Data Register (XRAM)

The chip contains a maximum of 256 bytes of XRAM, which is independent of the FLASH/RAM. The XRAM memory allocation block diagram is shown below:



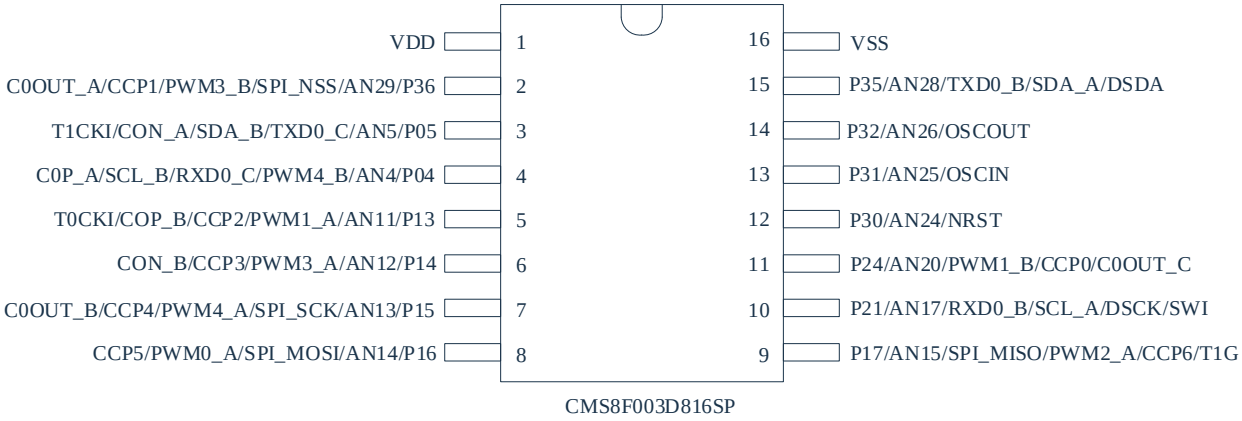
2.2.4 Special Function Register (XSFR)

XSFR is a special register that shares the addressing space with XRAM, primarily including the PWM function control registers. Its addressing range is shown in the diagram below:



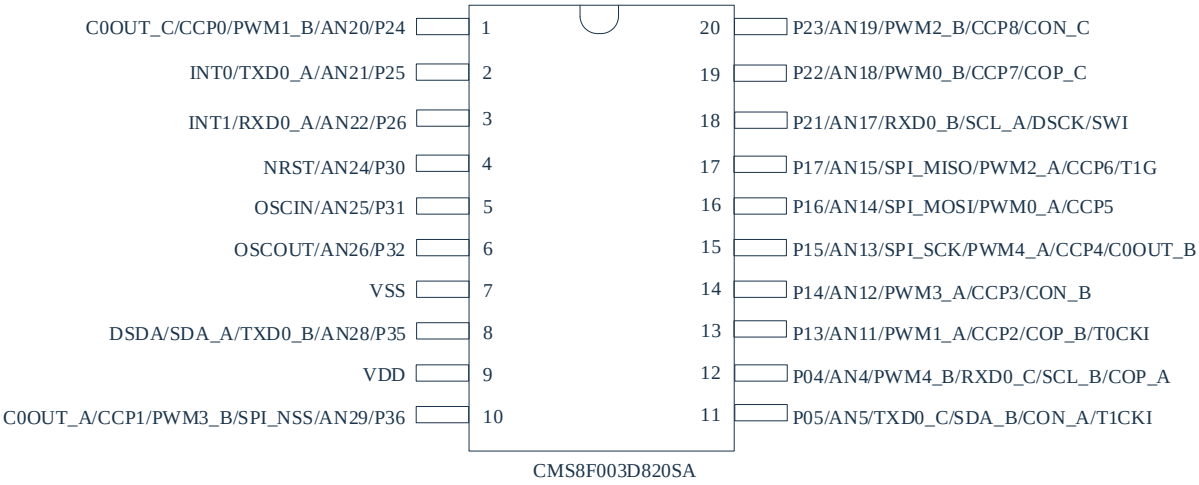
3. Pin Definition

3.1 CMS8F003D816SP



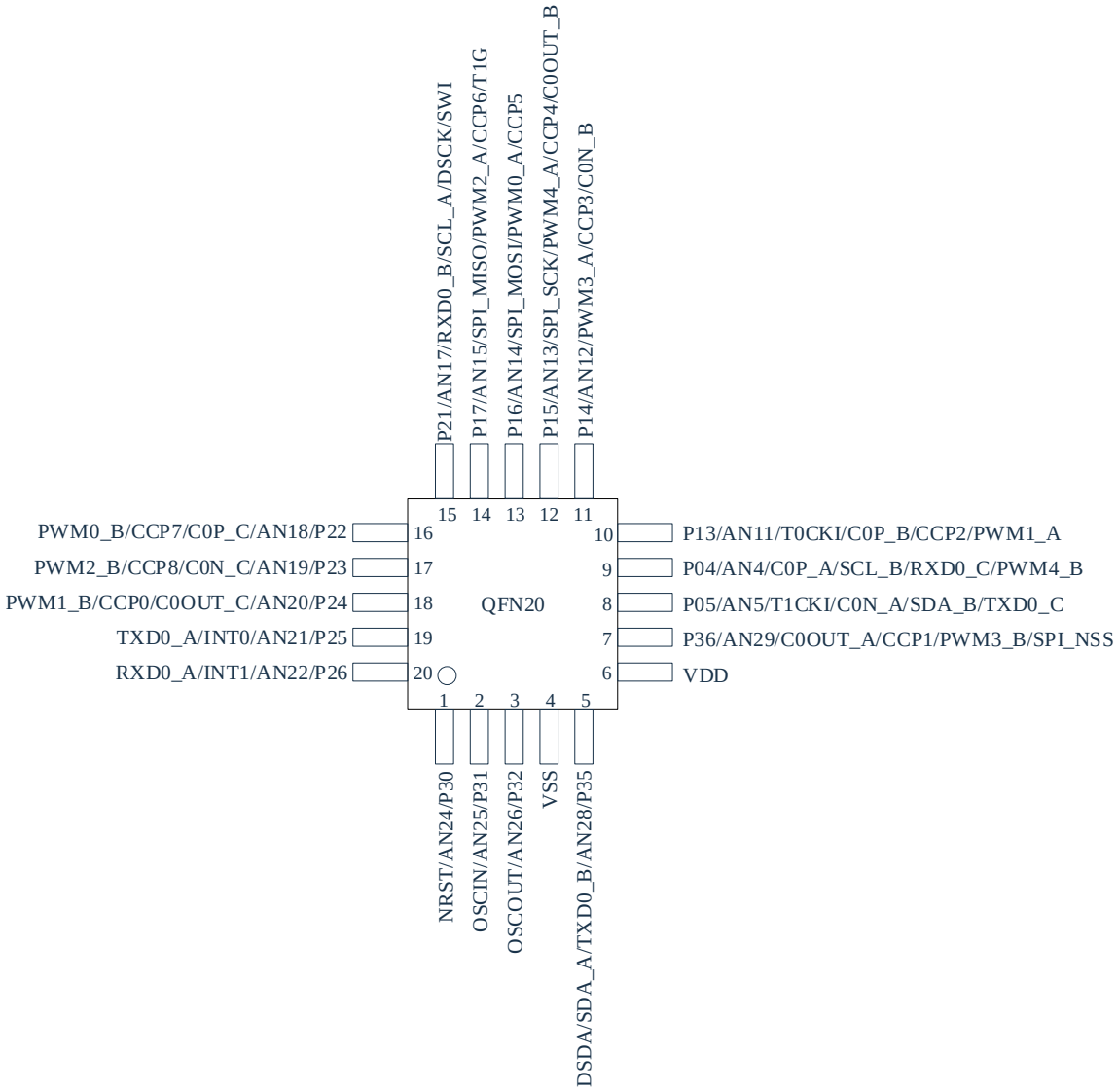
CMS8F003D816SP

3.2 CMS8F003D820SA



CMS8F003D820SA

3.3 CMS8F003D820NB



CMS8F003D820NB

Pin function description

Pin name	IO type	Description
VDD, GND	P	Power supply voltage input pin, ground pin
P04-P05	I/O	Programmable as input pin, push-pull output pin, with pull-up resistor, pull-down resistor, and open-drain output functionality
P13-P17	I/O	Programmable as input pin, push-pull output pin, with pull-up resistor, pull-down resistor, and open-drain output functionality
P21-P26	I/O	Programmable as input pin, push-pull output pin, with pull-up resistor, pull-down resistor, and open-drain output functionality
P30-P32, P35-P36	I/O	Programmable as input pin, push-pull output pin, with pull-up resistor, pull-down resistor, and open-drain output functionality
DSCK/ DSDA	I/O	Dual-wire debug programming clock/data pin
SWI	I/O	Single-wire debug communication port
AN0-AN29	I	12-bit ADC input pin
NRST	I	External reset input pin
INT0, INT1	I	External interrupt 0 and external interrupt 1 input pins
CCPx	I	Capture input pin
T0CKI	I	TIMER0 external clock input pin
T1CKI	I	TIMER1 external clock input pin
T1G	I	TIMER1 gate input pin
PWMn_X	O	PWM0-4 output pins
SCL_X	I/O	I^2C clock input/output pin
SDA_X	I/O	I^2C data input/output pin
TXD0_X	I/O	USART0 asynchronous transmission output/synchronous clock input/output pin
RXD0_X	I/O	USART0 asynchronous reception input/synchronous data input/output pin
OSCIN, OSCOUT	I	32.768K crystal oscillator input pin
C0P_X	I	Comparator positive input pin
C0N_X	I	Comparator negative input pin
C0OUT_X	O	Comparator result output pin
SPI_MISO	I/O	SPI master data input/slave data output pin
SPI_MOSI	I/O	SPI master data output/slave data input pin
SPI_SDIO	I/O	SPI three-wire mode data input/output pin
SPI_NSS	I	SPI slave mode enable input pin
SPI_SCK	I/O	SPI clock input/output pin

3.4 GPIO Features

The GPIO pins support multiple shared functions, with each I/O port configurable for any digital function or specified analog function. As general-purpose GPIO ports, they have the following features:

- Can read the data latch status or pin status.
- Configurable for interrupt triggering on rising edge, falling edge, or both edges.
- Configurable for interrupt wake-up on rising edge, falling edge, or both edges.
- Configurable as normal input, pull-up input, pull-down input, push-pull output, or open-drain output mode.

3.5 Pin Function List

The chip has four I/O ports: PORT0, PORT1, PORT2, and PORT3 (up to 18 I/Os). The port data registers can be read and written, allowing direct access to these ports.

Port	Bit	Function description	I/O
PORT0	4	Schmitt trigger input, push-pull output, AN4, RXD, SCL, PWM4, C0MP+	I/O
	5	Schmitt trigger input, push-pull output, AN5, TXD, SDA, T1CKI, COMP-	I/O
PORT1	3	Schmitt trigger input, push-pull output, AN11, PWM1, CCP2, COMP+, T0CKI	I/O
	4	Schmitt trigger input, push-pull output, AN12, PWM3, CCP3, COMP-	I/O
	5	Schmitt trigger input, push-pull output, AN13, SPI_SCK, PWM4, CCP4, COMPO	I/O
	6	Schmitt trigger input, push-pull output, AN14, SPI_MOSI, PWM0, CCP5	I/O
	7	Schmitt trigger input, push-pull output, AN15, SPI_MISO, PWM2, CCP6, T1G	I/O
PORT2	1	Schmitt trigger input, push-pull output, AN17, RXD, SCL, DSCK, SWI	I/O
	2	Schmitt trigger input, push-pull output, AN18, PWM0, CCP7, COMP+	I/O
	3	Schmitt trigger input, push-pull output, AN19, PWM2, CCP8, COMP-	I/O
	4	Schmitt trigger input, push-pull output, AN20, PWM1, CCP0, COMPO	I/O
	5	Schmitt trigger input, push-pull output, AN21, INT0, TXD	I/O
	6	Schmitt trigger input, push-pull output, AN22, INT1, RXD	I/O
PORT3	0	Schmitt trigger input, push-pull output, AN24, NRST	I/O
	1	Schmitt trigger input, push-pull output, AN25, OSCIN	I/O
	2	Schmitt trigger input, push-pull output, AN26, OSCOUT	I/O
	5	Schmitt trigger input, push-pull output, AN28, DSDA, SDA, TXD	I/O
	6	Schmitt trigger input, push-pull output, AN29, SPI_SS, PWM3, CCP1, COMPO	I/O

4. Function Summary

4.1 System Clock

The chip has two types of oscillation modes:

- Internal RC oscillation
- External XT oscillation

4.1.1 Internal RC Oscillation

The default oscillation mode of the chip is internal RC oscillation, with an oscillation frequency of 16 MHz. The chip's operating frequency can be set via the OSCCON register.

When the internal RC is selected as the chip's oscillator, the OSCIN and OSCOUT pins can be used as general-purpose I/O pins.

4.1.2 External XT Oscillation

When programming, set the OSC option in the CONFIG to XT. The chip operates in external XT oscillation mode, at which point the internal RC oscillation stops, and the OSCIN and OSCOUT pins function as oscillation pins.

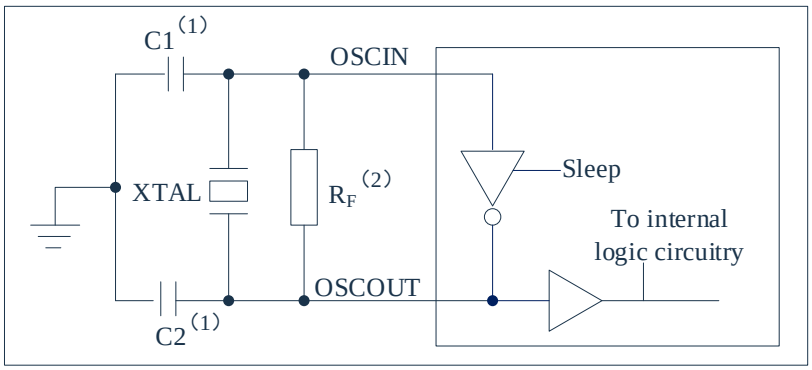


Figure 4-1: Typical XT oscillation mode

Recommended parameters:

Type	Frequency	Recommended value R_F	Recommended C1~C2 values
XT	4MHz	1MΩ	10pF~47pF
XT	8MHz	1MΩ	10pF~47pF
XT	16MHz	1MΩ	10pF~47pF

4.2 Reset

The chip can be reset in the following 4 ways:

- Power-on reset.
- Low voltage reset.
- Watchdog overflow reset during normal operation.
- External reset.

4.3 Power Management

4.3.1 Operating Modes

The chip has 3 different operating modes to suit the power consumption requirements of different applications.

- Normal operating mode: The MCU is in normal operation, and peripherals are functioning normally.
- Idle mode (IDLE): The MCU is in idle mode, the CPU stops working, and peripherals continue to run. This mode can be woken up by any interrupt.
- Sleep mode (STOP): The MCU is in sleep mode, both the CPU and peripherals stop working. This mode can be woken up by INT0/1 interrupts, GPIO interrupts, WUT timers, or LSE timers.

4.3.2 Low Voltage Reset (LVR)

When the power supply voltage falls below the set detection voltage, the system is reset. There are 4 options for low voltage reset: 1.8V, 2.0V, 2.5V, and 3.0V.

4.4 Interrupt Control

The chip has 17 interrupt sources and interrupt vectors:

Interrupt source	Interrupt description	Interrupt vector	Same-level priority sequence
INT0	External interrupt 0	0-0x0003	1
Timer0	Timer0 overflow interrupt	1-0x000B	2
INT1	External interrupt 1	2-0x0013	3
Timer1	Timer1 overflow interrupt	3-0x001B	4
TXIF	USART transmit interrupt	4-0x0023	5
RCIF	USART receive interrupt	5-0x002B	6
ADC	ADC interrupt	6-0x0033	7
PWM	PWM interrupt	7-0x003B	8
---	---	---	---
IIC	IIC interrupt	9-0x004B	10
BCLIF	IIC bus conflict interrupt	10-0x0053	11
CCP	CCP interrupt	11-0x005B	12
P0IF	PORT0 interrupt on change	12-0x0063	13
P1IF	PORT1 interrupt on change	13-0x006B	14
P2IF	PORT2 interrupt on change	14-0x0073	15
P3IF	PORT3 interrupt on change	15-0x007B	16
CMPIF	Comparator interrupt	16-0x0103	17
SPIIF	SPI interrupt	17-0x010B	18

The chip specifies two interrupt priority levels, allowing for two-level interrupt nesting. When one interrupt is being serviced, if a higher-priority interrupt request is received, the latter can preempt the former, achieving interrupt nesting.

4.5 Timers

4.5.1 WDT

The Watchdog Timer (WDT) is an on-chip timer that uses the system clock as its time source. A WDT overflow will trigger a reset. The watchdog reset serves as a protective mechanism for the system, allowing it to reset in case it enters an unknown state, thus preventing it from getting stuck in an infinite loop. The WDT timer has the following features:

- Eight selectable WDT overflow timing levels.
- Configurable watchdog overflow interrupt.
- Configurable watchdog overflow reset.

4.5.2 Timer0

TIMER0 consists of the following features:

- 8-bit Timer/Counter register (TMR0)
- 8-bit prescaler (shared with the Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Optional external 32.768K oscillator clock (F_{LSE})
- Overflow interrupt

4.5.3 Timer1

The TIMER1 module is a 16-bit timer/counter with the following features:

- 16-bit Timer/Counter register (TMR1H:TMR1L)
- 3-bit prescaler
- Synchronous or asynchronous operation
- Wake-up on overflow (only in external clock asynchronous mode)
- Programmable internal or external clock source
- Timer1 can be gated via the T1G pin (enabling/disabling counting)
- Overflow interrupt
- Capture/Compare functionality for time base

4.6 Enhanced Digital Peripherals

4.6.1 Capture Module (CCP)

The chip includes one capture module.

The capture module is a peripheral that allows the user to time and control different events. In capture mode, the peripheral can measure the duration of an event. Capture mode allows the user to trigger an external event after a predetermined timing period has elapsed.

4.6.2 PWM Module

The chip includes a 10-bit PWM module, which can be configured for 4 channels with a shared period and independent duty cycles, plus 1 independent output, or 2 complementary outputs with 1 independent output.

- Supports two waveform output modes: one-shot and continuous.
- Supports independent, complementary, and two-control modes.
- The counting clock can be selected with a prescaler of 1, 2, 4, 8, or 16.
- Supports dead-time programming.
- Output polarity can be set.

4.7 Communication Modules

4.7.1 USART Module

The UART has the following features:

- Full-duplex asynchronous transmission and reception
- Single-character output buffer
- Dual-character input buffer
- Frame error detection for received characters
- Half-duplex synchronous slave mode
- Programmable character length of 8 or 9 bits
- Input buffer overflow error detection
- Half-duplex synchronous master mode
- Programmable clock polarity in synchronous mode

4.7.2 SPI Module

The SPI mode allows simultaneous synchronous transmission and reception of 8-bit data. It supports both master and slave modes. Additionally, it can operate in either 3-wire or 4-wire mode.

SPI is a fully configurable SPI master/slave device, allowing users to configure the polarity and phase of the serial clock signal. SPI enables MCU communication with serial peripheral devices and can also facilitate inter-processor communication in multi-master systems. The SPI module has the following features:

- Full-duplex synchronous serial data transfer
- Supports master/slave mode
- Supports multi-master systems
- System error detection
- Supports speeds up to 1/4 of the system clock (F_{SYS}≤24 MHz)
- Interrupt generation upon completion of transmission/reception

4.7.3 I²C Module

The two-wire bidirectional serial bus controller I²C provides a simple and efficient connection for data exchange between a microprocessor and the I²C bus. The I²C module has the following features:

- Supports 4 operating modes: master transmission, master reception, slave transmission, slave reception.
- Supports 2 transfer speed modes: Standard (up to 100 Kb/s); Fast (up to 400 Kb/s).
- Performs arbitration and clock synchronization
- Supports multi-master systems
- In master mode, supports 7-bit and 10-bit addressing modes (software-supported)
- In slave mode, supports 7-bit addressing mode
- Operates over a wide clock frequency range (with built-in 8-bit timer)
- Interrupt generation upon completion of reception/transmission

4.8 Analog Modules

4.8.1 Analog-to-Digital Converter (ADC)

The Analog-to-Digital Converter (ADC) can convert analog input signals into a 12-bit binary number representing the signal. The device uses a shared sampling-and-holding circuit for all analog input channels. The output of the sampling-and-holding circuit is connected to the ADC input. The ADC uses a successive approximation method to generate a 12-bit binary result, which is stored in the ADC result register.

- Up to 18 external channels are supported.
- Four clock frequency options for ADC conversion.
- The ADC reference voltage can be selected as VDD/1.2V.
- A full 12-bit conversion requires 18 ADC conversion cycles.
- Interrupts are supported when the ADC conversion is completed.

4.8.2 Comparator (CMP)

The comparator outputs 1 when the positive input voltage is greater than the negative input voltage after digital filtering. Conversely, if the positive input voltage is less than the negative input voltage, the comparator outputs 0 after digital filtering.

- The comparator offset voltage is ≤±10mV.
- The input common-mode voltage range is 0V to VDD-1.3V.
- It includes an internal resistor voltage divider with a reference voltage of VDD.
- The comparator result can trigger an interrupt on either the rising or falling edge.
- The comparator result can be output through GPIO, with an option for reverse output.

4.9 Flash Memory

The Flash memory includes program memory (APROM/BOOT) and non-volatile data memory (Data FLASH), which can be accessed through the corresponding Special Function Registers (SFR) to enable In-Application Programming (IAP) functionality. Flash memory supports the following operations:

- Byte read operation.
- Byte write operation.
- Page erase operation.
- Flash space CRC operation.

5. User Configuration

The System Configuration Register (CONFIG) is used for setting the initial conditions of the MCU in Flash options. The program cannot access or modify this register. The following settings can be configured through the System Configuration Register:

- Watchdog operation mode.
- Flash program area partition protection, code encryption.
- Low voltage reset threshold.
- Debug mode enable or disable.
- Oscillation mode and pre-division selection.
- External reset pin pull-up function.

6. Electrical Characteristics

6.1 Limit Parameters

Supply voltage……GND-0.3V~GND+6.0V

Storage temperature…… -50℃~125℃

Working temperature……-40℃~85℃

Port input voltage……GND-0.3V~V_{DD}+0.3V

Maximum positive current for all ports…… 200mA

Maximum negative current for all ports……-150mA

Note: If the device operating conditions exceed the above “limit parameters”, it may cause permanent damage to the device. The above values are extreme values for the operating conditions, and we do not recommend that the device be operated outside of the range specified in this specification. The stability of the device will be affected if it is operated for a long period of time under extreme conditions.

6.2 DC Characteristics

(VDD=5V, T_A= 25°C, unless otherwise specified)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
VDD	Operating voltage	-	F_{SYS}=16MHz/2T	V_{LVR2}	-	5.5	V
		5V	F_{SYS}=16MHz/2T, all analog modules OFF	-	4	-	mA
		3V	F_{SYS}=16MHz/2T, all analog modules OFF	-	2	-	mA
		5V	Program EEPROM	-	6	-	mA
I_{STB}	Static current	5V	LVR=DIS WDT=DIS	-	1.5	5	uA
		3V	LVR=DIS WDT=DIS	-	0.6	3	uA
		5V	LVR=DIS WDT=EN	-	4.8	12	uA
		3V	LVR=DIS WDT=EN	-	2.1	5.5	uA
V_{IL}	Low level input voltage	-	----	-	-	0.3VDD	V
V_{IH}	High level input voltage	-	----	0.7VDD	-	-	V
V_{OH}	High level output voltage	-	No load	0.9VDD	-	-	V
V_{OL}	Low level output voltage	-	No load	-	-	0.1VDD	V
V_{EEPROM}	EEPROM module operating voltage	-	----	2.5	-	5.5	V
R_{PH}	Pull-up resistor value	5V	Vo=0.5VDD	-	36	-	KΩ
		3V	Vo=0.5VDD	-	56	-	KΩ
R_{PL}	Pull-down resistor value	5V	Vo=0.5VDD	-	36	-	KΩ
		3V	Vo=0.5VDD	-	60	-	KΩ
I_{OL}	Output pin sink current	5V	V_{OL}=0.3VDD	-	40	-	mA
		3V	V_{OL}=0.3VDD	-	20	-	mA
I_{OH}	Output pin source current	5V	V_{OH}=0.7VDD	-	-20	-	mA
		3V	V_{OH}=0.7VDD	-	-10	-	mA
V_{BG}	Internal reference voltage 1.2V	VDD=2.5~5.5V T_A=25°C		-1.5%	1.2	+1.5%	V
		VDD=2.0~5.5V T_A=25°C		-2.5%	1.2	+2.5%	V
		VDD=2.5~5.5V T_A=-40~85°C		-2.0%	1.2	+2.0%	V
		VDD=2.0~5.5V T_A=-40~85°C		-3.0%	1.2	+3.0%	V

6.3 Comparator Characteristics

(TA= 25℃, unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD	Operating voltage range	-	2.0	-	5.5	V
Iwork	Operating current	VDD=5V COMP+=2V COMP-=2V	-	34	46	uA
		VDD=3V COMP+=1V COMP-=1V	-	20	26	uA
I_{BG}	BG operating current	VDD=5V	-	35	46	uA
		VDD=3V	-	33	44	uA
V_{IN}	Input common-mode voltage range	-	0	-	VDD-1.3	V
Vos	Offset voltage	-	-	-	±13	mV
LSB	Minimum resolution	-	-	10	20	mV
Tr	Response time	-	-	-	6	us
-	Internal resistance divider error	VDD=5V V_R>1V	-1%	-	+ 1%	-
		VDD=5V V_R<1V	-2%	-	+ 2%	-

Remark: V_R is the output value of the internal resistor voltage divider.

6.4 ADC Electrical Characteristics

(T_A= 25℃, unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{ADC}	ADC operating voltage	V_{ADREF}= VDD, F_{ADCCLK}=1MHz	3.0		5.5	V
		V_{ADREF}= VDD, F_{ADCCLK}=500kHz	2.7		5.5	V
		V_{ADREF}=2.0V, F_{ADCCLK}=250kHz	2.7		5.5	V
		V_{ADREF}=2.4V, F_{ADCCLK}=250kHz	2.7		5.5	V
		V_{ADREF}=3.0V, F_{ADCCLK}=500kHz	3.3		5.5	V
I_{ADC}	ADC conversion current	V_{ADC}=5V, V_{ADREF}= VDD, F_{ADCCLK}=500kHz			500	uA
		V_{ADC} =3V, V_{ADREF}= VDD, F_{ADCCLK}=500kHz			200	uA
V_{AIN}	ADC input voltage	V_{ADC}=5V, V_{ADREF} = VDD, F_{ADCCLK}=500kHz	0		V_{ADC}	V
DNL1	Differential non-linearity error	V_{ADC}=5V, V_{ADREF} = VDD, F_{ADCCLK}=1MHz		±4		LSB
INL1	Integral non-linearity error	V_{ADC}=5V, V_{ADREF} = VDD, F_{ADCCLK}=1MHz		±8		LSB
DNL2	Differential non-linearity error	V_{ADC}=5V, V_{ADREF} = 3.0V, F_{ADCCLK}=500kHz,V_{AIN}<1V		±4		LSB
INL2	Integral non-linearity error	V_{ADC}=5V, V_{ADREF} = 3.0V, F_{ADCCLK}=500kHz,V_{AIN}<1V		±16		LSB
DNL3	Differential non-linearity error	V_{ADC}=5V, V_{ADREF} = 2.4V, F_{ADCCLK}=250kHz,V_{AIN}<0.8V		±4		LSB
INL3	Integral non-linearity error	V_{ADC}=5V, V_{ADREF} = 2.4V, F_{ADCCLK}=250kHz,V_{AIN}<0.8V		±16		LSB
DNL4	Differential non-linearity error	V_{ADC}=5V, V_{ADREF} = 2.0V, F_{ADCCLK}=250kHz,V_{AIN}<0.7V		±4		LSB
INL4	Integral non-linearity error	V_{ADC}=5V, V_{ADREF} = 2.0V, F_{ADCCLK}=250kHz,V_{AIN}<0.7V		±16		LSB
T_{ADC}	ADC conversion time			16		T_{ADCCLK}

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.5 Power-On Reset Characteristics

(T_A= 25℃, unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{VDD}	VDD rising rate	-	0.05	-	-	V/ms
V_{LVR1}	LVR set voltage=1.8V	VDD=1.6~5.5V	1.7	1.8	1.9	V
V_{LVR2}	LVR set voltage=2.0V	VDD=1.8~5.5V	1.9	2.0	2.1	V
V_{LVR3}	LVR set voltage=2.5V	VDD=2.3~5.5V	2.4	2.5	2.6	V
V_{LVR4}	LVR set voltage=3.0V	VDD=2.8~5.5V	2.9	3.0	3.1	V

6.6 AC Electrical Characteristics

(T_A= 25℃, unless otherwise specified)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
F_{WDT}	WDT clock source	VDD=2.5~5.5V	T_A=25℃	-20%	32	+20%	KHz
		VDD=1.8~5.5V	T_A=25℃	-30%	32	+30%	KHz
		VDD=2.5~5.5V	T_A=-40~85℃	-30%	32	+30%	KHz
		VDD=1.8~5.5V	T_A=-40~85℃	-50%	32	+50%	KHz
T_{EEPROM}	EEPROM programming time	5V	F_{HSI}=16MHz	-	4.6	-	ms
		3V	F_{HSI}=16MHz	-	4.6	-	ms
F_{INTRC}	Internal oscillator frequency 16MHz	VDD=4.0~5.5V	T_A=25℃	-1.5%	16	+1.5%	MHz
		VDD=2.5~5.5V	T_A=25℃	-2.0%	16	+2.0%	MHz
		VDD=1.8~5.5V	T_A=25℃	-3.0%	16	+3.0%	MHz
		VDD=4.0~5.5V	T_A=-40~85℃	-2.5%	16	+2.5%	MHz
		VDD=2.5~5.5V	T_A=-40~85℃	-3.5%	16	+3.5%	MHz
		VDD=1.8~5.5V	T_A=-40~85℃	-5.0%	16	+5.0%	MHz

6.7 LSE Characteristics

(T_A= 25℃, unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD	Operating voltage range	-	1.8	-	5.5	V
F_{LSE}	LSE ocillation frequency	-	-	32.768	-	KHz
C1	OSCIN pin matching capacitance	-	-	22	-	pF
C2	OSCOUT pin matching capacitance	-	-	22	-	pF
I_{LSE}	LSE operating current	VDD=5V C_1=22pF C_2=22pF	-	20	-	uA
		VDD=3V C_1=22pF C_2=22pF	-	8	-	uA
T_{LSE}	LSE stabilization time	VDD=5V C_1=22pF C_2=22pF	-	260	700	ms
		VDD=3V C_1=22pF C_2=22pF		300	1000	ms

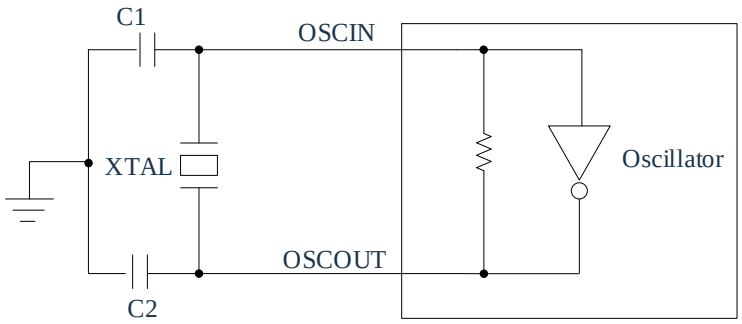


Figure 6-1: Typical application circuit

6.8 IIC Electrical Characteristics

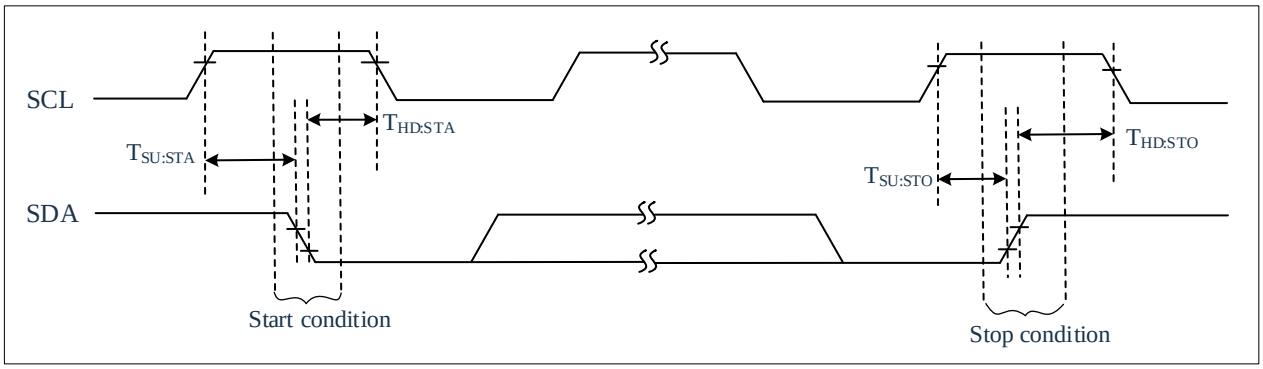


Figure 6-2: I²C™ bus start/stop bit timing

Symbol	Feature		Condition	Min.	Typ.	Max.	Unit
$T_{SU:STA}$	Start condition setup time	100kHz mode	Related only to the repeated start condition.	4700	-	-	ns
		400kHz mode		600	-	-	ns
$T_{HD:STA}$	Start condition hold time	100kHz mode	The first clock pulse is generated after this period.	4000	-	-	ns
		400kHz mode		600	-	-	ns
$T_{SU:STO}$	Stop condition setup time	100kHz mode		4700	-	-	ns
		400kHz mode		600	-	-	ns
$T_{HD:STO}$	Stopt condition hold time	100kHz mode		4000	-	-	ns
		400kHz mode		600	-	-	ns

Remark: These parameters are guaranteed by characterization results and are not tested.

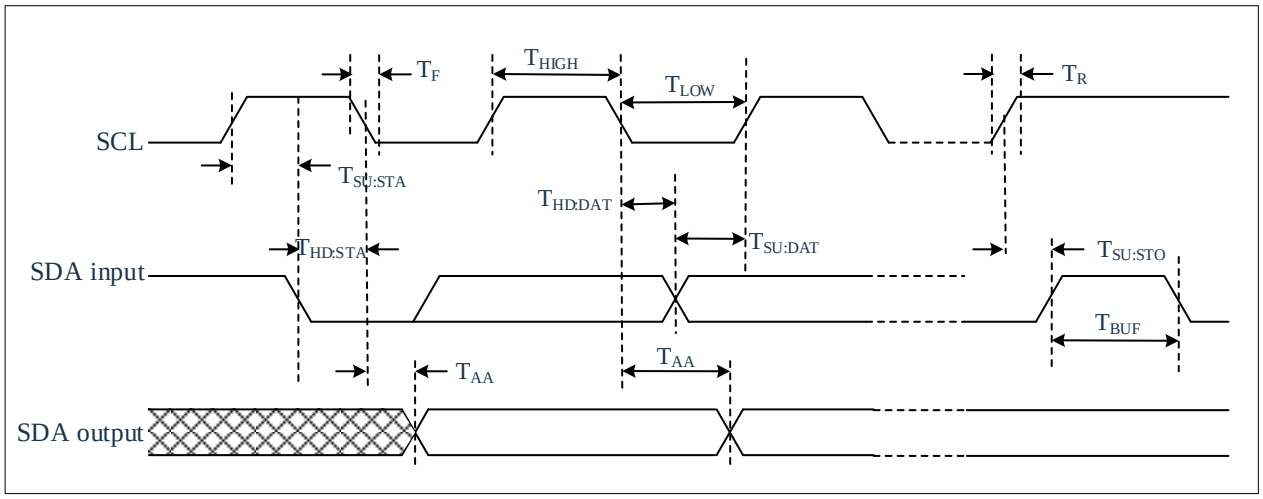


Figure 6-3: I²C™ bus data timing

Symbol	Feature		Condition	Min.	Max.	Unit
T_{HIGH}	Clock high level time	100kHz mode	The device operating frequency must not be lower than 4MHz.	4.0	-	us
		400kHz mode	The device operating frequency must not be lower than 16MHz.	0.6	-	us
T_{LOW}	Clock low level time	100kHz mode	The device operating frequency must not be lower than 4MHz.	4.7	-	us
		400kHz mode	The device operating frequency must not be lower than 16MHz.	1.3	-	us
T_R	SDA and SCL rise time	100kHz mode		-	1000	ns
		400kHz mode	The C_B value is specified between 10-400pF.	20+0.1C_B	300	ns
T_F	SDA and SCL fall time	100kHz mode		-	300	ns
		400kHz mode	The C_B value is specified between 10-400pF.	20+0.1C_B	300	ns
$T_{SU:STA}$	Start condition setup time	100kHz mode	Only related to the repeated start condition.	4.7	-	us
		400kHz mode		0.6	-	us
$T_{HD:STA}$	Start condition hold time	100kHz mode	The first clock pulse is generated after this period.	4.0	-	us
		400kHz mode		0.6	-	us
$T_{HD:DAT}$	Data input hold time	100kHz mode		2/F_{sys}	-	us
		400kHz mode		2/F_{sys}	1-2/F_{sys}	us
$T_{SU:DAT}$	Data input setup time	100kHz mode		2/F_{sys}	-	us
		400kHz mode		2/F_{sys}	-	us
$T_{SU:STO}$	Stop condition setup time	100kHz mode		4.7	-	us
		400kHz mode		0.6	-	us
T_{AA}	Clock output valid time	100kHz mode		-	3.7-2/F_{sys}	us
		400kHz mode		-	-	us

T_{BUF}	Bus idle time	100kHz mode	The bus must remain idle for a certain time before starting a new transfer.	4.7	-	us
		400kHz mode		1.3	-	us
C_B	Bus capacitance load			-	400	pF

Remark: These parameters are guaranteed by characterization results and are not tested.

6.9 EMC Characteristics

6.9.1 EFT Electrical Characteristics

Symbol	Parameter	Test condition	Grade
V_{EFTB}	Fast transient voltage burst limits to be applied through 0.1μF (capacitance) on VDD and VSS pins to induce a functional disturbance	T_A = + 25℃, F_{SYS}=8MHz, conforms to IEC 61000-4-4	4

Note: The immunity performance against Electrical Fast Transient (EFT) pulses is closely related to system design aspects, including power supply structure, circuit design, layout and wiring, chip configuration, program structure, and more. The EFT parameters listed in the table are results obtained from testing on CMS internal testing platforms and may not apply universally to all application environments. These test data serve as reference only. Various aspects of system design can influence EFT performance. In applications where high EFT immunity is required, it is advisable to design while minimizing the impact of interference sources on system operation. It is recommended to analyze interference paths and optimize designs to achieve the best immunity performance against EFT disturbances.

6.9.2 ESD Electrical Characteristics

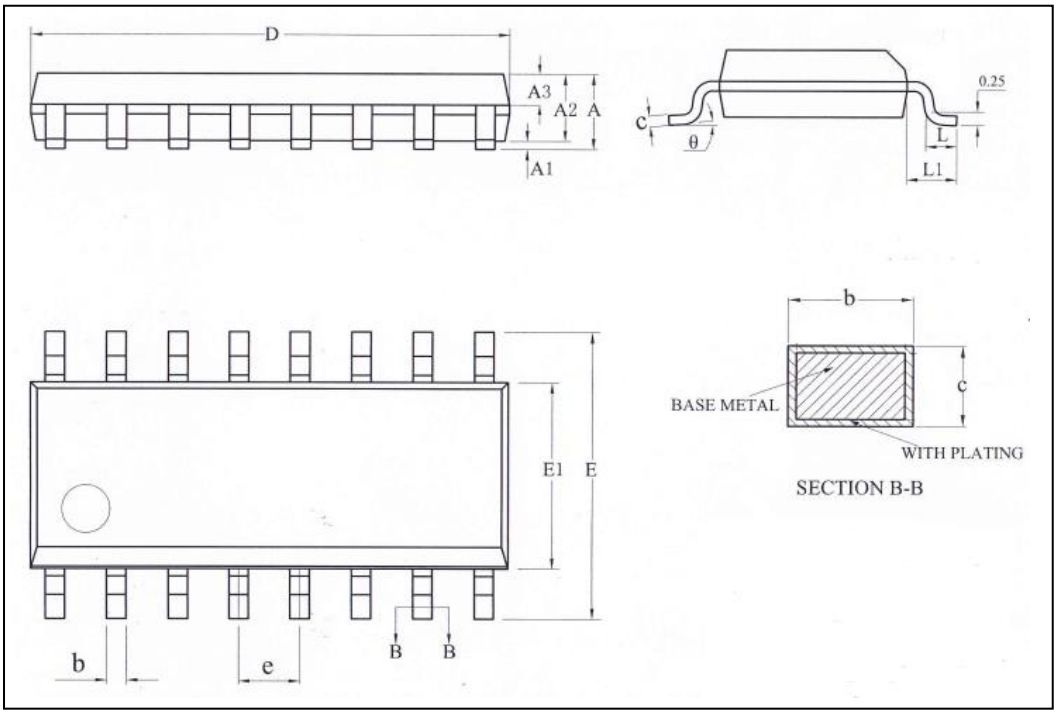
Symbol	Parameter	Test condition	Grade
V_{ESD}	Electrostatic discharge (Human-Body Model: HBM)	T_A = + 25℃, ANSI/ESDA/JEDEC JS-001-2023	Class 2
	Electrostatic discharge (Charged-Device Model: CDM)	T_A = + 25℃, ANSI/ESDA/JEDEC JS-002-2022	C3

6.9.3 Latch-Up Electrical Characteristics

Symbol	Parameter	Test condition	Classification
LU	Static latch-up	JSED 78F.01:2022	Class I.A (T_A = +25℃)

7. Package Dimensions

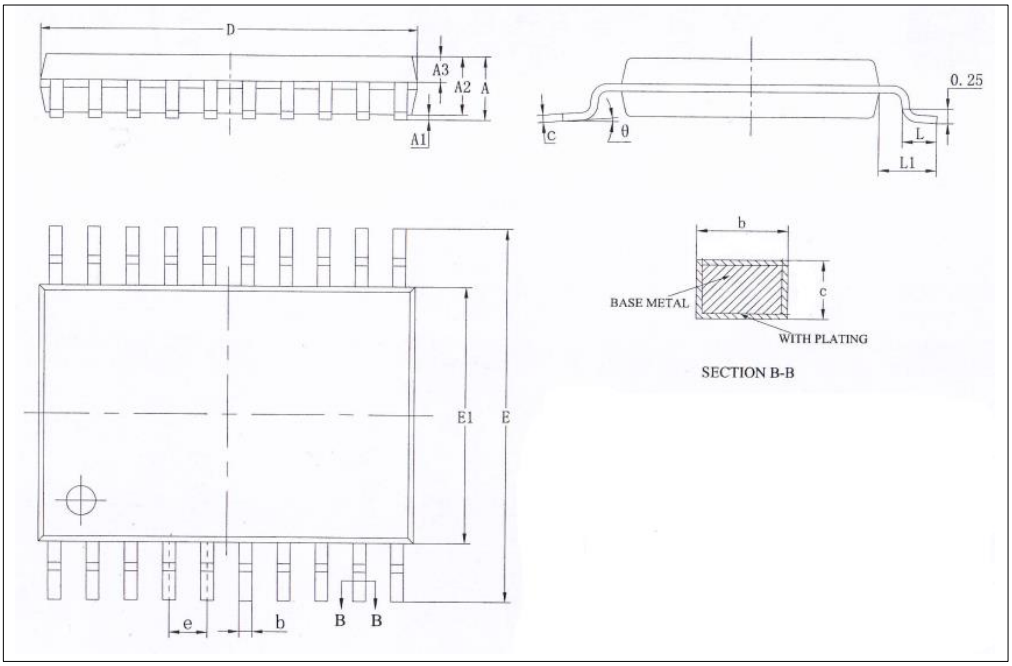
7.1 SOP16



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.85
A1	0.05	-	0.25
A2	1.30	-	1.60
A3	0.60	-	0.71
b	0.356	-	0.51
c	0.20	-	0.26
D	9.70	-	10.10
E	5.80	6.00	6.20
E1	3.70	-	4.10
e	1.27BSC		
h	0.25	-	0.50
L	0.40	-	0.80
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

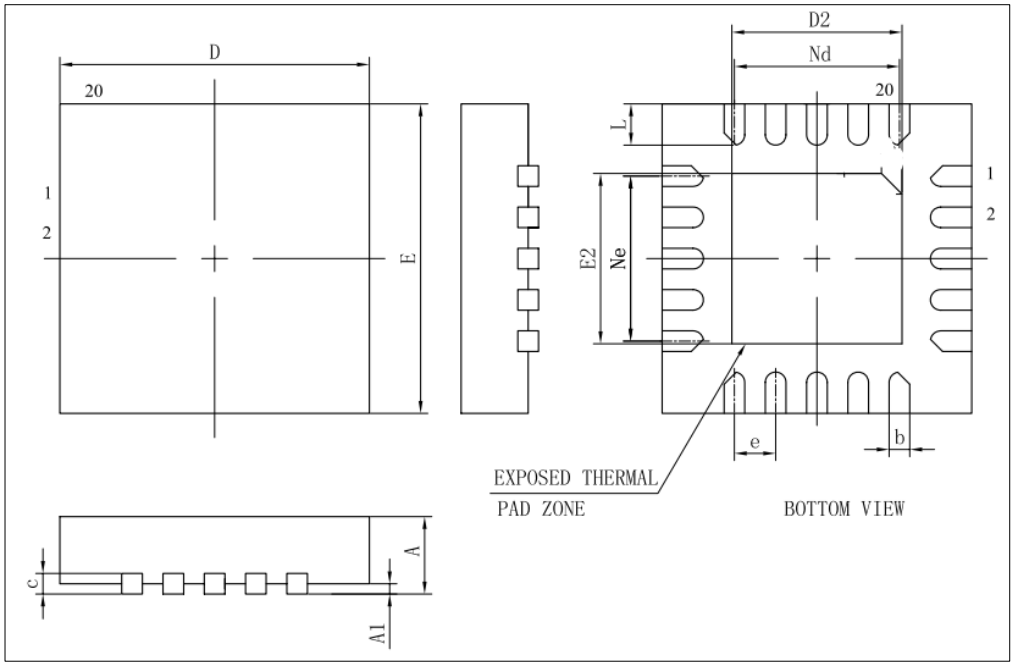
7.2 TSSOP20



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.25
A1	0.05	-	0.15
A2	0.80	1.00	1.10
A3	0.34	0.44	0.54
b	0.20	-	0.28
c	0.10	-	0.19
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

7.3 QFN20 (3*3*0.75-0.40mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.65	0.75	0.85
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	-	2.00
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	-	2.00
L	0.20	-	0.50

Caution: Package dimensions do not include mold flash or gate burrs.

8. Version History

Version #	Date	Description of changes
V0.1.0	Nov. 2024	Initial release
V0.1.1	Dec. 2024	Updated parameters in Section 6.2
V0.9.0	Feb. 2025	Updated Product Model List
V0.9.1	Apr. 2025	1. Corrected the electrical parameters of the product 2. Removed Section 1.3 Online Serial Programming 3. Updated the content of Section 2.1 System Overview 4. Added Section 2.2.4 Special Function Registers (XSFR) and reclassified the Function Summary section. 5. Removed the Unique ID section
V0.9.2	May 2025	1. Removed the description of the 1T instruction 2. Added a section on EMC Characteristics
V0.9.3	May 2025	Added the model CMS8F003D820NB and its package dimensions
V0.9.4	June 2025	Corrected 16MHz/2T operating voltage range
V0.9.5	Aug 2025	1. Delete the FLASH data protection description in the user configuration area 2. Add the CMS8F003D816SP model and its package